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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/602,300	06/23/2000	G. Eric Engstrom	3382-55510	1178

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EXAMINER
PATEL, HARESH N

ART UNIT	PAPER NUMBER
2126	6

DATE MAILED: 09/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/602,300	ENGSTROM ET AL.	
	Examiner	Art Unit	
	Haresh Patel	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-10 and 20 are presented for examination.

Priority

2. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged.

Drawings

3. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

4. An initialed and dated copy of Applicant's IDS form 1449, Paper No. 3, is attached to the instant Office action.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 20 is rejected under 35 U.S.C. 102(b) as being anticipated by applicant's admitted prior art (AAPA).

As per claim 20, AAPS teaches the following:

a computer-readable medium (e.g., memory, page 1, line 23) having stored thereon a data structure (e.g., segment register, page 4, line 27) comprising:

a series of data fields representing blocks of code or data associated with an application to be treated as a single unit for purposes of virtual memory management (e.g. One form of virtual memory in common use today is referred to as paged virtual memory. In a paged virtual memory scheme, the operating system carries out all memory allocation, de-allocation, and swapping operations in units of memory called pages, page 4, lines 4-10), the data fields including a list of memory addresses of the blocks and sizes of each block in the list; (e.g., With paging enabled, the processor maps this address in virtual memory space to an address in physical memory space. Figure 1 is a diagram illustrating how the processor interprets the 32-bit address from an application. The top 10 bits (31 .. 22) (see 20 in Fig. 1) are an index into a page table directory (22 in Fig. 1). Part of each 32-bit quantity in a page table directory points to a page table (24 in Fig. 1), page 5, lines 19 – 27)

wherein the data structure is evaluated in a data processing operation to load each of the blocks into physical memory whenever a not-present interrupt is generated for any memory address referring to a location included in one of the blocks (e.g., if an access to that code or data is attempted, the processor will generate a not present interrupt that notifies the operating system of the problem, page 2, lines 22-25, the term page fault" refers to an interrupt generated by a microprocessor indicating that the memory request cannot be satisfied from physical memory because the page containing the requested code or data is not located in physical memory, page 4, lines 15-18).

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Maund et al. 5,611,064 (Hereinafter Maund).

9. As per claims 1 and 10, Maund teaches the following:

in a multitasking operating system that uses virtual memory to share physical memory among concurrently executing application programs, a method for controlling allocation of physical memory comprising,

a computer-readable medium storing instructions for performing:

in response to a call from an application program (e.g., application) other than an operating system, to groupspecified code or data in a group (e.g., groups referred to as `pages`, col. 9, lines 51-60), creating a structure to group the code or data specified by the application (e.g., In turn, as illustrated in FIG. 7A, the patches are arranged in 32.times.32 groups referred to as `pages`. Furthermore, as illustrated in FIG. 7B, the pages are arranged in 4.times.4 groups referred to as `superpages`, col. 9, lines 51 – 60),

monitoring for a not-present interrupt generated in response to request to access any part of the code or data in the group (e.g., In this case the processor means is preferably operable in response to the group fault signal to determine whether there is any available location in the

CAM, and if not to select a virtual group component to delete from the CAM, and to determine whether any pages of data-elements of the selected group are stored in the second memory, and if so to cause the transfer means to transfer those pages of data-elements from the second memory to the first memory, col. 2, lines 53 – 67),

when the not-present interrupt occurs for a unit of memory in the group (e.g., fault signal, col. 2, lines 53 – 67), loading all of the code or data in the group that is not already in physical memory into physical memory from secondary storage at one time (e.g., determining whether any of the pages within the selected group are stored in second memory and if so transferring those pages from second memory to first memory, col. 2, lines 18-68, col. 9, line 44 – col. 12. line 68), including loading the unit of memory for which the not present interrupt has occurred and all other units of memory used to store the code or data in the group (e.g., determining whether any of the pages within the selected group are stored in second memory and if so transferring those pages from second memory to first memory, col. 2, lines 18-68, col. 9, line 44 – col. 12. line 68).

10. As per claims 2-9, Maund teaches the following:

the structure includes a linked list structure that links together code or data stored at non-contiguous portions of virtual memory (e.g., In this case the processor means is preferably operable in response to the group fault signal to determine whether there is any available location in the CAM, and if not to select a virtual group component to delete from the CAM, and to determine whether any pages of data-elements of the selected group are stored in the second

memory, and if so to cause the transfer means to transfer those pages of data-elements from the second memory to the first memory, col. 2, lines 53 – 67),

the structure links pages of memory associated with the non-contiguous portions of code or data (e.g., In this case the processor means is preferably operable in response to the group fault signal to determine whether there is any available location in the CAM, and if not to select a virtual group component to delete from the CAM, and to determine whether any pages of data-elements of the selected group are stored in the second memory, and if so to cause the transfer means to transfer those pages of data-elements from the second memory to the first memory, col. 2, lines 53 – 67),

for additional groups of code or data specified by the application (e.g., In this case the processor means is preferably operable in response to the group fault signal to determine whether there is any available location in the CAM, and if not to select a virtual group component to delete from the CAM, and to determine whether any pages of data-elements of the selected group are stored in the second memory, and if so to cause the transfer means to transfer those pages of data-elements from the second memory to the first memory, col. 2, lines 53 – 67),

for another concurrently executing application such that more than one concurrently executing application program has specified at least one group of code or data to be treated as a single piece of memory for loading into physical memory in response to a not-present interrupt (e.g., if an access to that code or data is attempted, the processor will generate a not present interrupt that notifies the operating system of the problem, page 2, lines 22-25, the term page fault" refers to an interrupt generated by a microprocessor indicating that the memory request

cannot be satisfied from physical memory because the page containing the requested code or data is not located in physical memory, page 4, lines 15-18),

when the not-present interrupt occurs, checking whether the interrupt has occurred for a unit of memory in the group by evaluating whether an address of the memory request for which the interrupt occurred is within a series of non-contiguous memory addresses of the group (e.g., if an access to that code or data is attempted, the processor will generate a not present interrupt that notifies the operating system of the problem, page 2, lines 22-25, the term page fault" refers to an interrupt generated by a microprocessor indicating that the memory request cannot be satisfied from physical memory because the page containing the requested code or data is not located in physical memory, page 4, lines 15-18),

tracking memory accesses to units of memory in the group together such that when a unit of memory in the group is accessed (e.g., means to keep track of the pages, col. 1, lines 48 – 62), all of the units of memory in the group are marked as accessed (e.g., means to keep track of the pages, col. 1, lines 48 – 62), and determining which portions of physical memory to swap from physical memory to secondary storage by determining which units of code are marked as accessed, such that units are selected to be swapped from physical memory to secondary storage based on frequency of use or how recently the units of code have been accessed (e.g., As a result, pages which are contiguous in the virtual memory address space are not necessarily stored contiguously in the second memory address space, and it is therefore necessary to provide a means to keep track of the pages in the second memory and to translate between the virtual page address and the corresponding second memory page address, col. 1, lines 48 –62),

in response to a call from an application program to group specified code or data in a second group (e.g., whether any pages of data-elements of the selected group are stored in the second memory, col. 2, lines 53 – 67), creating a second structure to group the code or data specified by the application (e.g., whether any pages of data-elements of the selected group are stored in the second memory, col. 2, lines 53 – 67), tracking memory accesses to units of memory in the first and second group such that when a unit of memory in both the first and second group is accessed, all of the units of memory in the first and second group are marked as accessed and the unit of memory in both the first and second group is marked as being accessed twice (e.g., In this case the processor means is preferably operable in response to the group fault signal to determine whether there is any available location in the CAM, and if not to select a virtual group component to delete from the CAM, and to determine whether any pages of data-elements of the selected group are stored in the second memory, and if so to cause the transfer means to transfer those pages of data-elements from the second memory to the first memory, col. 2, lines 53 – 67),

when a block of code or data shared between two or more groups is accessed (e.g., pages aligned across several bank addresses, col. 11, line 61 – col. 12. line 47), marking the block as being accessed n times where n is the number of groups that share the block (e.g., pages aligned across several bank addresses, col. 11, line 61 – col. 12. line 47).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haresh Patel whose telephone number is (703) 605-5234. The examiner can normally be reached on Monday-Friday from 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee, can be reached at (7 03) 305-8498.

The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) 306-5404.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Haresh Patel

September 2, 2003.

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100